PRELIMINARY DATA SHEET

ARX-01

FPGA-controlled 1550 nm APD optical receiver and pulse-modulation front-end

Preliminary engineering data sheet | Revision A | August 2026

DEVICE ROLE A SYZYGY optical receiver peripheral that converts low-level APD pulses into a 12-bit source-synchronous ADC stream and a parallel fast-comparator event signal for Artix-7 FPGA processing.

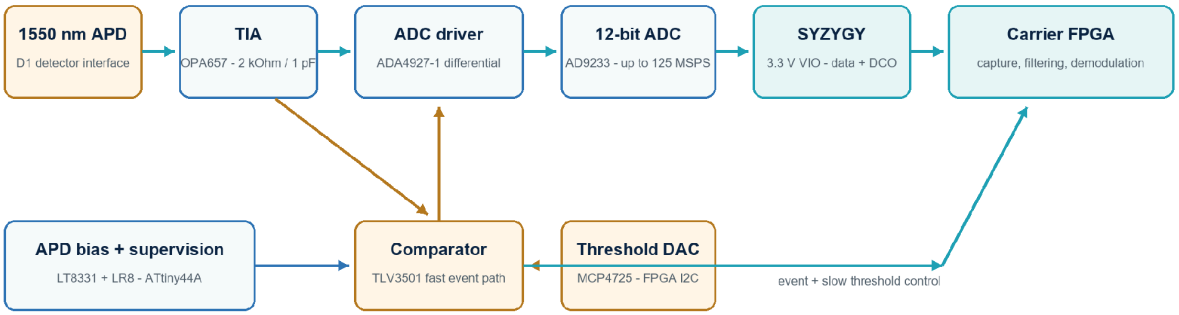

Figure 1. Functional signal path. Illustration is not a mechanical drawing.

Key capabilities

- **12-bit digitization:** AD9233 parallel ADC, operated up to 125 MSPS.
- **Raw sample payload:** 1.50 Gbit/s at 125 MSPS before framing, coding, decimation or metadata overhead.
- **Dual receive paths:** ADC samples for soft decisions plus a TLV3501 comparator event path for low-latency detection.
- **FPGA-adjustable threshold:** MCP4725 DAC controlled through a dedicated 100 kbit/s-or-slower I^2C bus.
- **FPGA-defined modulation:** OOK and multiple PPM families can be decoded without changing the analog board.
- **Supervised APD bias:** adjustable LR8 post-regulator with ATtiny-controlled high-voltage enable and bias monitoring.

Supported transmission and receive formats

The board is an optical receiver front-end. It can receive the formats below when the carrier FPGA implements the matching clock recovery, framing, decision logic and decoder, and when a compatible optical transmitter generates the waveform. These are programmable system capabilities, not fixed hardware modem modes.

Format	Bits / symbol	Optical symbol	FPGA receive method
OOK	1	Pulse present or absent in a bit period	Threshold or matched-filter decision per bit period
2-PPM	1	One pulse in 2 slots	Select the strongest / valid slot
4-PPM	2	One pulse in 4 slots	Resolve one of four slot indices
8-PPM	3	One pulse in 8 slots	Resolve one of eight slot indices
16-PPM	4	One pulse in 16 slots	Resolve one of sixteen slot indices
32-PPM	5	One pulse in 32 slots	Resolve one of thirty-two slot indices
64-PPM	6	One pulse in 64 slots	Resolve one of sixty-four slot indices
Differential PPM	Scheme-dependent	Position change relative to the prior symbol	Decode relative timing; retain previous-symbol state
Multipulse PPM	$\log_2 C(M,k)$*	k pulses selected among M slots	Detect multiple valid peaks and map the slot combination
Variable / guarded PPM	Scheme-dependent	Unequal slots and/or explicit guard time	Use a programmable slot schedule and guard validation

** C(M,k) is the number of k-pulse combinations available within M slots; practical mappings may reserve combinations for framing or error control.*

Figure 2. Representative receive timing patterns; pulse widths and slot ratios are illustrative.

Receiver architecture and FPGA interface

Interface	SYZYGY pin(s)	Function
ADC data	J1.5-J1.17*	Twelve 3.3 V LVCMOS ADC bits in a non-sequential connector order; capture using DCO.
ADC overrange	J1.13	Active-high overrange aligned with the ADC output word.
Comparator event	J1.18	Buffered active-high event input for hard-decision or timestamp logic.
Threshold DAC	J1.19 SCL / J1.20 SDA	Dedicated open-drain MCP4725 control bus with 4.7 kΩ pull-ups to VIO.
AVDD power-good	J1.21	TPS746 open-drain status; synchronize before use.
ADC data clock	J1.33	Single-ended 3.3 V source-synchronous DCO.
Sample clock	J1.34 CLK+ / J1.36 CLK-	Carrier-to-peripheral differential ADC clock. J1.35 is unused.
VIO	J1.39	Must be 3.3 V for this build.

** ADC bit order is not connector order. Assemble {D11..D0} from {J1.12, J1.17, J1.11, J1.10, J1.16, J1.9, J1.15, J1.8, J1.14, J1.7, J1.6, J1.5}.*

Preliminary electrical characteristics

Parameter	Current build / design intent
Detector interface	1550 nm InGaAs APD footprint and high-voltage bias path
TIA feedback	2.0 kΩ with 1 pF feedback capacitor; final bandwidth requires board measurement
ADC	AD9233BCPZ-125, 12-bit CMOS parallel output, 125 MSPS maximum
ADC supply / power	1.8 V AVDD; 1.8 V to 3.3 V DRVDD; approximately 395 mW typical at 125 MSPS under ADI reference conditions
ADC format	Two's-complement in the current hardware strap configuration
Raw ADC payload	1.50 Gbit/s at 125 MSPS (125 MSPS x 12 bits); DCO, overrange and protocol overhead are additional
Threshold control	12-bit MCP4725 DAC; intended control rate 100 kbit/s or slower
Comparator	TLV3501 fast comparator followed by a VIO-powered tri-state buffer
APD bias range	Approximately 39.4 V to 69.7 V nominal, manually adjusted
Normal D1 limit	65 V maximum continuous default until the individual detector VOP and qualification data are available
VIO	3.3 V required

FPGA implementation guidance

- Use DCO for source-synchronous capture and constrain every ADC bit plus OR relative to J1.33.
- Implement pulse detection with a selectable ADC-based soft metric, comparator events, or a combination of both.
- For PPM, make slot width, frame length, guard time, detection threshold and expected pulse count programmable.
- For differential PPM, retain prior-symbol timing state and define resynchronization behavior after a missing or invalid pulse.
- For multipulse PPM, explicitly handle collisions, missing pulses and reserved slot combinations.
- Do not infer a guaranteed modulation rate from the 125 MSPS ADC limit; the APD, TIA, pulse shape, optical power, jitter and FPGA algorithm set the usable rate.

QUALIFICATION STATUS This is a preliminary engineering data sheet. Maximum optical data rate, sensitivity, dynamic range, pulse-pair resolution, false-alarm rate, APD operating voltage and thermal limits require measurement on assembled hardware. The current PCB design also requires routing and production-rule closure before manufacturing release.

Recommended validation for each modulation mode

Characterize minimum detectable pulse energy, timing error, false-alarm probability, adjacent-slot leakage, maximum count rate and recovery after overload. Repeat at the selected APD bias, across temperature, and with both comparator and ADC-based decisions.

System integration, power and cooling

ARX-01 is intended to operate as a SYZYGY receiver peripheral connected to a Digilent USB104 A7 carrier using the AMD Artix-7 XC7A100T FPGA. The carrier captures the 12-bit ADC bus and DCO, performs pulse detection and demodulation, buffers samples, and applies mission-selected framing and channel coding.

Supply / subsystem	Requirement or design intent
USB104 A7 carrier input	Regulated 5 V; use an external supply capable of at least 5 A. The supplied/recommended 5 V, 6 A, 30 W adapter provides margin for FPGA operation and attached peripherals.
USB-only carrier input	Limited to approximately 2 A by the carrier load switch; not recommended for the complete receiver and cooling assembly.
SYZYGY fixed rails	Carrier capability: up to 1.5 A at 5 V and 1.0 A at 3.3 V for the USB104 A7 standard port.
SYZYGY VIO	3.3 V required by this ARX-01 build; USB104 A7 VIO capability is up to 1.0 A across its programmable 1.2 V to 3.3 V range.
Receiver power budget	Verify measured current on every rail and retain 20% to 30% system margin before design release.
Peltier/TEC supply	Use a dedicated, current-limited supply and TEC driver sized from the selected module data; do not route TEC current through the SYZYGY connector.

Peltier-effect front-end cooling

A thermoelectric cooler may stabilize the APD and TIA region to reduce temperature-dependent dark current, noise and gain drift. Couple the TEC cold side to the detector/front-end thermal interface and conduct heat from the hot side into a rated heat sink with forced airflow. A thermistor located near the detector should close the temperature-control loop. The controller should enforce current limiting, soft start, overtemperature shutdown and a lower setpoint limit that prevents condensation. The enclosure design must provide insulation and moisture management whenever the front end operates below ambient temperature.

ESTOL and CCSDS design alignment

COMPLIANCE POSITION ARX-01 is designed to support ESTOL- and CCSDS-aligned development. It is not presently certified or formally compliant. ARX-01 is a receiver peripheral, while ESTOL compliance applies to the complete optical terminal and air interface.

Area	ARX-01 implementation intent	Status
ESTOL physical layer	1550 nm receiver front end, digitization and FPGA-configurable receive processing; terminal-level wavelength, sensitivity, modulation, FEC, BER and PAT requirements remain profile dependent.	Design alignment; test required

Area	ARX-01 implementation intent	Status
CCSDS synchronization	For a selected conventional non-turbo TM profile, the FPGA can prepend/detect the 32-bit Attached Synchronization Marker 0x1ACFFC1D, MSB first.	Planned in FPGA
CCSDS framing	Fixed-length transfer frames with protocol ID, frame counters, timestamp, rate identifier, sample count, receiver status, payload and error-control field.	Architecture defined
Channel coding	Randomization, CRC, Reed-Solomon, LDPC or other coding is selected by the mission profile; the ASM and coding chain must match the applicable CCSDS recommendation.	Profile selection pending
Verification	Requirement traceability, FPGA vector tests, optical characterization, BER testing and interoperability with a recognized reference terminal.	Required for compliance claim

Receiver-to-FPGA data definition

- **ADC transport:** 12 data bits, source-synchronous DCO and overrange at up to 125 MSPS.
- **Raw payload rate:** 1.50 Gbit/s before protocol and coding overhead.
- **Required metadata:** sampling rate, configured output rate, timestamp, valid-sample count, gain/threshold settings, temperature, saturation and fault flags.
- **Frame synchronization:** use the ASM required by the selected CCSDS coding profile; 0x1ACFFC1D is not universal to every CCSDS mode.

Reference documents

- Analog Devices, AD9233 12-Bit, 80/105/125 MSPS ADC Data Sheet, Rev. B: https://www.analog.com/media/en/technical-documentation/data-sheets/ad9233.pdf
- Digilent, USB104 A7 Hardware Reference Manual: https://digilent.com/reference/programmable-logic/usb104a7/reference-manual
- Opal Kelly, SYZYGY Specification v1.1.1 and SYZYGY DNA Specification v1.1: https://syzygyfpga.io/specification/
- ESA, Specification for Terabit/s Optical Links (ESTOL): https://resilience.esa.int/artes-4-0-programme-overview/optical-quantum-communications-scylight/estol-esa-specifications-for-terabit-sec-optical-links
- CCSDS, TM Synchronization and Channel Coding and applicable mission profile: https://ccsds.org/searchpubs/